Bluetooth Headset IC - WS9621NLSE

Datasheet

Version: V1.3, January 2013

110/F 530 Tower, QingYuan Road, TaiHu International Technology Park,
WuXi New District, 214135, China
Tel：86-510-81816000
Fax: 86-510-81816935
Web: www.vimicro.com

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OVERVIEW

WS9621NLSE is a stereo headset version solution based on Bluetooth protocol. It consists of ARM CM3 processor, SRAM, via ROM, Bluetooth baseband controller, MODEM, RF, Audio CODEC, PMU, etc. The protocol stack is stored in the via ROM. It supports all the mandatory features of Bluetooth version 3.0+EDR.

FEATURES

- Supports all mandatory Bluetooth v3.0 + EDR features including eSCO and AFH.
- Allows full speed data transfer, mixed voice and data, and full piconet operation, including all EDR packet types.
- Audio transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air.
- Good performance for RF Characteristics.
- Dual Microphone inputs.
- Advanced Audio arithmetic to improve quality of voice and music.
- Powered by 3.0-5.5V Li-Ion battery, charged by 3.0-6.5V Adapter or USB.
- Internal PMU for total Chip power solution.1.2V core, 3.3V I/O.
- UART interface with programmable baud rate up to 3Mbaud for HCI communication.
- Multiple I^2C interfaces for external EEPROM.
- Internal 32KHz oscillator for low power operation.
- QFN48 package.
- Crystal oscillator with frequency 13-52MHz.

TYPICAL APPLICATION

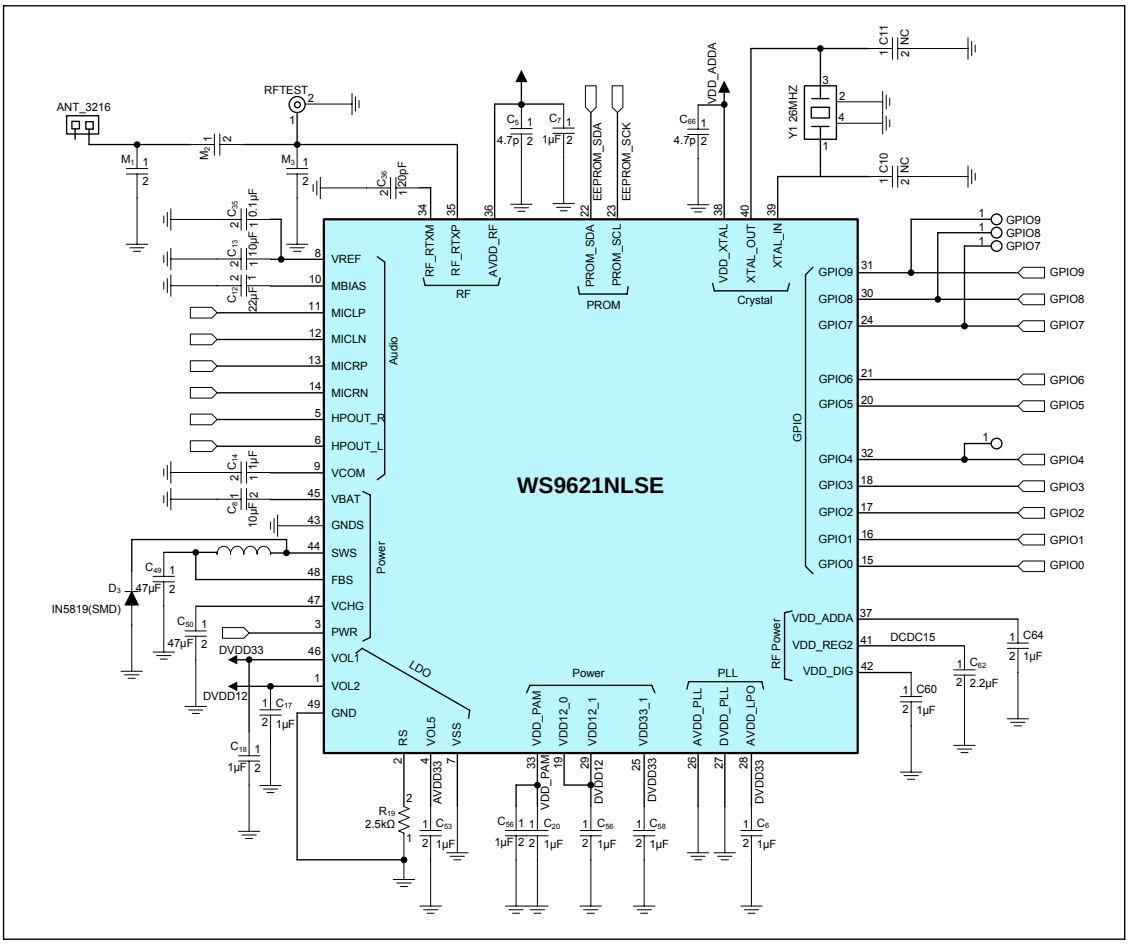


Figure 1 WS9621NLSE Typical Application

PIN CONFIGURATIONS

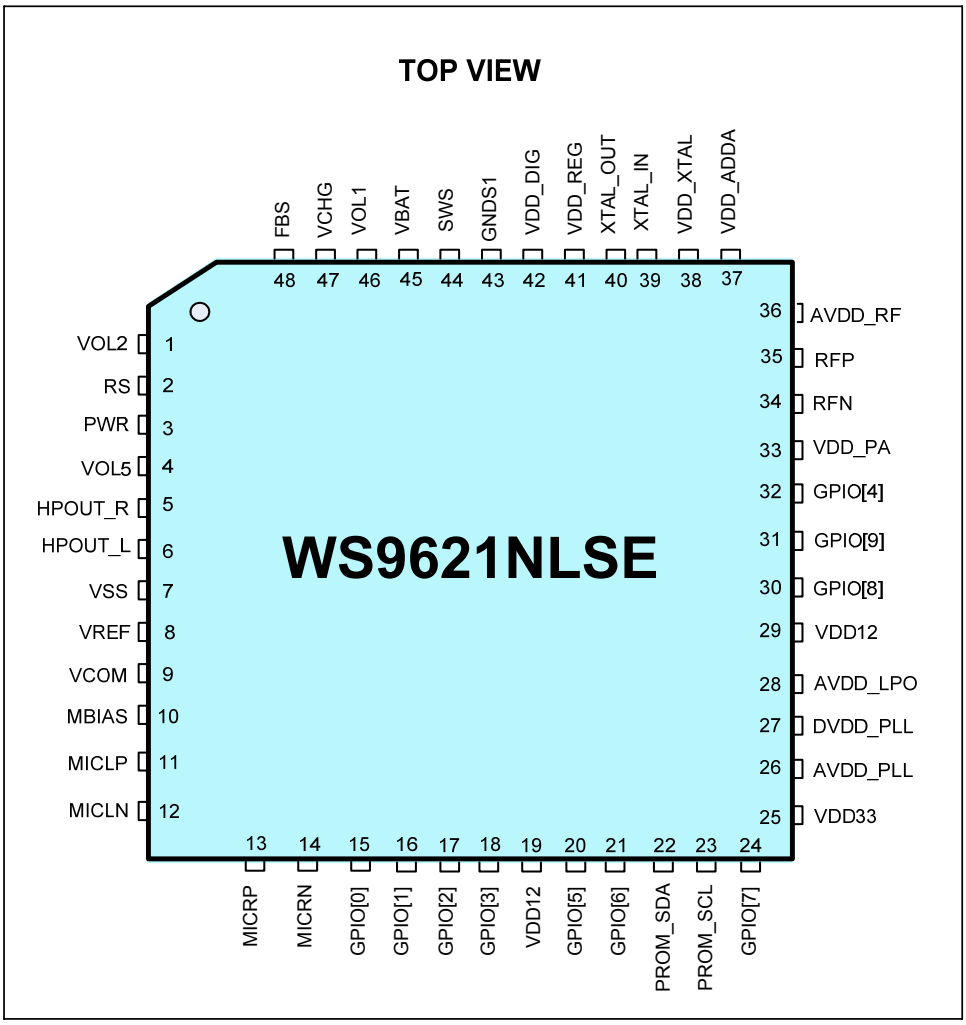


Figure 2 WS9621NLSE Pin Assignment (Not to scale)

PIN DESCRIPTION

[Table 1] Pin Descriptions by Oder

ORDER	PIN NAME	DIR	POWER	DESCRIPTION
1	VOL2	AIO	AVDDBAT	LDO2 (1.2V) output. Power supply of core of digital logic.
2	RS	AI	AVDDBAT	Set charging current.
3	PWR	AI	AVDDBAT	Power up reset, High level (BAT voltage) means button is turned on
4	VOL5	AIO	AVDDBAT	LDO5 (3.3V) output. Power supply for Audio an HP (AVDD33 power domain).
5	HPOUT_R	A,O	AVDD33	Headphone right channel output.
6	HPOUT_L	A,O	AVDD33	Headphone left channel output.
7	VSS	P	AVDD33	Ground for Audio.
8	VREF	AIO	AVDD33	Internal reference voltage output.
9	VCOM	AIO	AVDD33	Common mode reference voltage.
10	MBIAS	A,O	AVDD33	Microphone bias voltage output, tied 2.2μF capacitor to AVSS.
11	MICLP	A,I	AVDD33	Microphone left channel input, positive end.

ORDER	PIN NAME	DIR	POWER	DESCRIPTION
12	MICLN	A,I	AVDD33	Microphone left channel input, negative end.
13	MICRP	A,I	AVDD33	Microphone right channel input, positive end.
14	MICRN	A,I	AVDD33	Microphone right channel input, negative end.
15	GPIO[0]	B	VDD33	General purpose IO.
16	GPIO[1]	B	VDD33	General purpose IO.
17	GPIO[2]	B	VDD33	General purpose IO.
18	GPIO[3]	B	VDD33	General purpose IO.
19	VDD12_1	P	DVDD12	Digital core power.
20	GPIO[5]	B	VDD33	General purpose IO.
21	GPIO[6]	B	VDD33	General purpose IO.
22	PROM_SDA	B	VDD33	EEROM interface: I^2C data signal.
23	PROM_SCL	B	VDD33	EEROM interface: I^2C clock signal.
24	GPIO[7]	B	VDD33	General purpose IO.
25	VDD33	P	DVDD33	Digital I/O power.
26	AVDD_PLL	P	DVDD12	PLL IP power.
27	DVDD_PLL	P	DVDD12	PLL IP power.
28	AVDD_LPO	P	DVDD33	LPO power.
29	VDD12_2	P	DVDD12	Digital core power
30	GPIO[8]	B	VDD33	General purpose IO
31	GPIO[9]	B	VDD33	General purpose IO
32	GPIO[4]	B	VDD33	General purpose IO
33	VDD_PA	P,O	AVDD125	PA supply. LDO output, connect to decoupling capacity.
34	RFN	AIO	AVDD125	RF input/output, drive SAW filter. Require on board matching network.
35	RFP	AIO	AVDD125	RF input/output, drive SAW filter, Require on board matching network.
36	AVDD_RF	P	AVDD125	RF front end supply. LDO output, connect to decoupling capacity.
37	VDD_ADDA	P	AVDD125	Analog V_{DD}, LDO output, connect to decoupling capacity.
38	VDD_XTAL	P	AVDD125	XTAL V_{DD}, LDO output, connect to decoupling capacity.
39	XTAL_IN	AIO	AVDD125	XTAL input, connect to crystal capacity.
40	XTAL_OUT	AIO	AVDD125	XTAL output, connect to crystal capacity.
41	VDD_REG	P,I	AVDD15	XTAL/Analog/RF ido power (1.5V) input, external power supply from FBS. Need 3.3μF and 4.7pF on board capacity.
42	VDD_DIG	P	AVDD125	Digital V_{DD}, LDO output, connect to decoupling capacity.
43	GNDS1	P	AVDDBAT	Ground of switching Buck DC-DC.
44	SWS	AIO	AVDDBAT	Connect the inductor of switching Buck DC-DC.
45	VBAT	P, IO	AVDDBAT	Battery positive terminal.
46	VOL1	AIO	AVDDBAT	LDO1 (3.3V) output and input for POR. Power supply of digital I/O (DVDD33 power domain).
47	VCHG	P, I	AVDDBAT	Charger input terminal.
48	FBS	AIO	AVDDBAT	Feedback pin of switching Buck DC-DC. Source of AVDD 15 power domain.

[Table 2] Pin Numbers by Interface

INTERFACE	PIN NUMBER
EEPROM Interface	22, 23
GPIO Interface	15~18, 20, 21, 24, 30~32
PMU Interface	1~4, 7~9, 19, 25~29, 33, 36~38, 41~48
Audio Interface	5, 6, 10~14
Radio Interface	34, 35
Crystal Interface	39, 40

Note 1:

P	Power/Ground
A	Analog
I	Input
O	Output
B	Bi-direction
PP	Internal programmable pull up/down
Sch	Schmitt Input

FUNCTIONAL BLOCK DESCRIPTION

Radio Transceiver

The WS9621NLSE has an integrated radio transceiver that has been optimized for 2.4 GHz Bluetooth wireless systems. It has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification 3.0 and EDR specification, and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

The WS9621NLSE features a fully integrated zero-IF transmitter. The baseband transmits GFSK, DQPSK, 8DPSK data that is digitally modulated in the modem block, and then up-converts the data to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filters, I/Q up-converters, output Power Amplifiers (PAs), and RF filters. The digital modulator performs the data modulation and filtering required for the GFSK, DQPSK, and 8-DPSK signals. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

Receiver Path

The receiver path uses a low-IF architecture to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The front-end topology with built-in out-of-band attenuation enables the WS9621NLSE to be used in most applications with no off-chip filtering. The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm. The radio portion of the WS9621NLSE also provides a Received Signal Strength Indication (RSSI) signal to the baseband so that the controller can participate in a Bluetooth power-controlled link.
the interfaces to and from the RF and Baseband.

Baseband

The Baseband performs all the bit-level and packet processing required in Bluetooth. The transmitter module constructs a packet based on the information contained in registers which configured by ARM and transmit to Modem. The receiver decodes the information in the received packet from Modem and updates the related registers in the register file and data buffer to be read and processed by ARM.

These functions contain the interfaces to and from the RF and Modem.

ARM

The Cortex M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARMv7-M architecture.

The CM3 on this Chip implement many functions below: runs the Bluetooth software stacks; performs the complex Audio arithmetic to improve quality of voice and music; controls the peripherals on chip and etc.

Audio codec

Audio Codec includes two channel voice band 16bit ADC which can support stereo microphone recording, two channel CD quality 24bit Audio DACs, one microphone bias output, two 40mW headphone PAs.

Power Management

PMU is an integrated power solution for applications powered by one small Li-Ion battery. It provides total power solution for WS9621. It provides one highly efficient, low output ripple step-down converter to provide the core voltage. Step-down converter enters PFM mode at light load for maximum efficiency over the widest possible range of load currents. The PMU also integrates three LDO regulators (with Charger bypass mode), POR, Start-up controller and a battery charger. The charger block will provide smart battery charging management while LDO will provide a low-noise power supply for WS9621. POR will provide reset signal for digital core.

SRAM

The SRAM of 128kB is used in WS9621NLSE Chip. This memory stores the data generated or required by running CM3.

ROM

The VIA ROM of 512KB is employed in WS9621NLSE Chip. This memory is used to store the firmware.

DEVICE TERMINAL DESCRIPTIONS

Power Supply

WS9621NLSE is powered by one small Li-Ion battery via the pins VBAT and GNDS1. The voltage value range of battery is from 3.0V to 5.5V.

It can be connected to charger via the pin VCHG, the charger block will provide smart battery charging management and power supply through LDO for chip simultaneously. The Input voltage of charger is from 3.0V to 6.5V (From Adapter or USB).

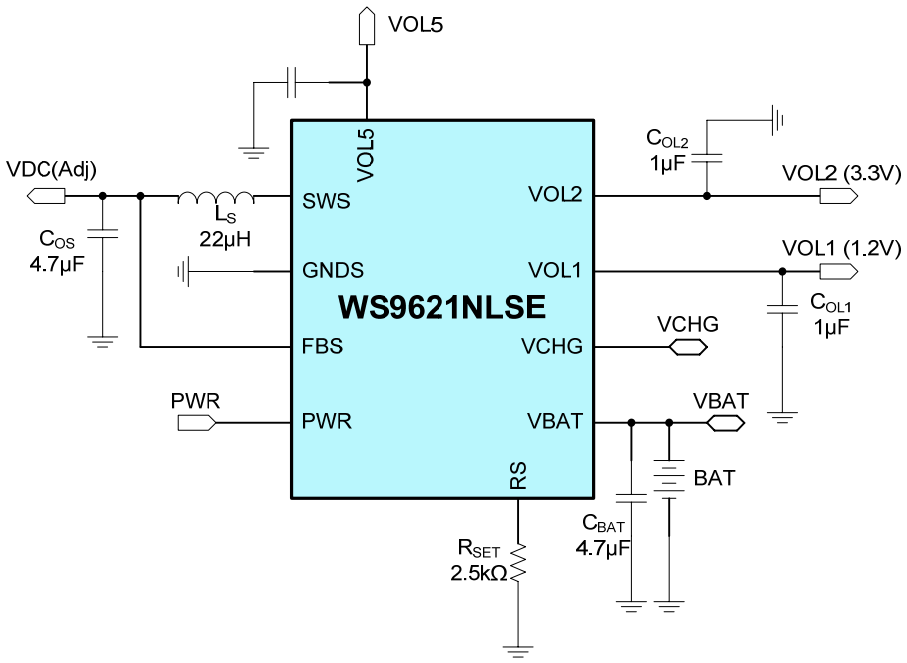


Figure 3 WS9621NLSE Typical Power Application

Cristal Oscillator

Port XTAL_IN and XTAL_OUT need to be bonded out and connect to the on-board crystal circuit. The load cap for both pins is 4-12pF. The on-board crystal circuit needs to be placed close to the chip. The on-chip DCXO circuit can work with crystal frequency from 13 to 52MHz.

The initialization time for the DCXO circuit to settle to 20ppm accuracy is 2mS. The reference clock generated by the DCXO goes to RFPLL and DPLL. However, the reference clock generated by DCXO can be directly feed to the digital baseband in that case.

The on-chip DCXO circuit has a cap tuning array that can be used to trim reference clock frequency.

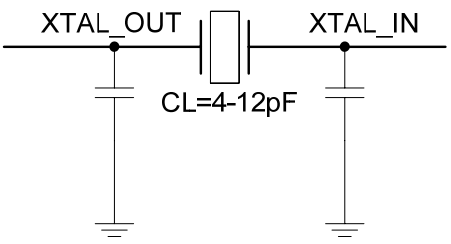


Figure 4 Typical Application of XTAL_IN and XTAL_OUT

RF Interface

Port RFP and RFN are the RF I/O ports. They need to be bonded out. The two RF pins connect to on-board matching network, which should be placed close to the chip and the associated on–board transmission line routing should have 50Ω impedance matching.

Audio Interface

WS9621NLSE has Dual Microphone Audio inputs. The port MICLP and MICLN are microphone left channel inputs, differential inputs. The port MICRP and MICRN are microphone right channel inputs, differential inputs.

The stereo Audio output ports are HPOUTL and HPOUTR. Where, HPOUTL is headphone left channel output while HPOUTR is headphone right channel output.

UART Interface

General Description

The UART (Universal Asynchronous Receiver/Transmitter) core provides serial communication capabilities, which allow communication with external devices, like another computer using a serial cable and RS232 protocol. The UART module performs all of the normal operations associated with start-stop asynchronous communication. Serial data is transmitted and received at standard bit rates using the internal baud rate generator. This core is designed to be maximally compatible with the industry standard National Semiconductors' 16550A device (The Modem interface and feature is not included).

Followings are the main features of UART IP core:

- Full-duplex operation
- Robust receiver data sampling with noise filtering
- 32-byte FIFO for receive, 32-byte FIFO for transmit
- 7-bit or 8-bit operation with optional parity
- Break generation and detection
- Baud rate generator
- Support up to 3Mbps.baud rate with 16x sample clock
- Integer and fractional divisor for baud rate.
- Hardware flow control
- Loop-back mode for self test

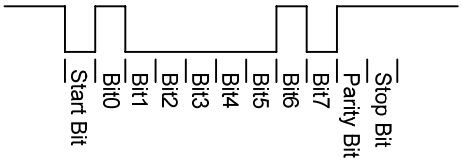
The UART ports are shared with GIPO[3:0]. Those ports are used as UART by configuring related register by SW.

Function Description

Serial Operation

The UART module has one operation modes --- non-return to zero (NRZ).

The NRZ mode is primarily associated with RS-232. Each character is transmitted as a frame delimited by a start bit at the beginning and a stop bit at the end. Data bits are transmitted least significant bit first, and each bit occupies a period of time equal to 1 full bit. If parity is used, the parity bit is transmitted after the most significant bit. Following is the waveform in NRZ mode.



NRZ mode transmits a ASCII "A" Character with Odd

Figure 5 Waveform of UART

UART External Connection for Bluetooth

The UART in WS9621NLSE can be used to transport HCI (Host Controller Interface) packets for Bluetooth. The HCI UART Transport Layer uses the following settings for RS232:

Baud rate	manufacturer-specific
Number of data bits	8
Parity bit	no parity
Stop bit	1 stop bit
Flow control	RTS/CTS (Hardware Flow Control)
Flow-off response time	manufacturer specific

The RS232 signals should be connected in a null-modem fashion.

The most expensive null modem cable is the null modem cable suitable for full handshaking. In this null modem cable, seven wires are present. Only the ring indicator RI and carrier detect CD signal are not linked. The cable is shown in the following figure. DTR and DSR are not used in UART of WS9621NLSE.

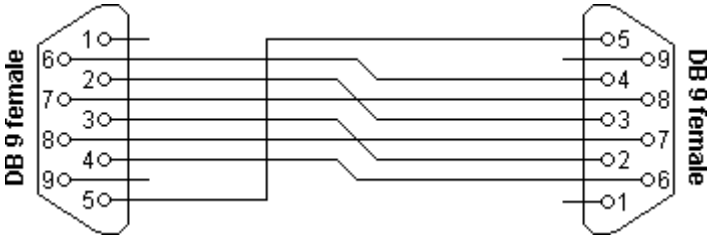


Figure 6 Null Modem Cable Connection

Connector 1	Connector 2	Function		
2	3	Rx	←	Tx
3	2	Tx	→	Rx
4	6	DTR	→	DSR
5	5	Signal ground		
6	4	DSR	←	DTR
7	8	RTS	→	CTS
8	7	CTS	←	RTS

In CTS/RTS flow, The RTS output of device1 signals device2 that device1 is capable of receiving information. The device2 will send the data out when the RTS signal of device1 is set valid. Also, the device1 will send the data out when the RTS signal of device2 is set valid.

I²C Interface

WS9621NLSE provides the two ports, PROM_SCL and PROM_SDA, for communication with EEPROM which comply with I²C protocol.

I²C is a two-wire, bi-directional serial bus, which provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

The interface defines 2 transmission speeds:
- Normal: 100Kbit/s
- Fast: 400Kbit/s

Only 100Kbps and 400Kbps modes are supported directly.

FEATURES:
- Compatible with I^2C standard;
- Multi Master Operation;
- Supports 7 and 10bit addressing mode;
- Software programmable clock frequency, supports a wide range of input clock frequencies;
- Software programmable acknowledge bit;
- Interrupt or bit-polling driven byte-by-byte data-transfers;
- Arbitration lost interrupt, with automatic transfer cancellation;
- Bus busy detection;
- Clock Stretching and Wait state generation;

Interface Timing Signal with I^2C bus

System Configuration

The I^2C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (sees START and STOP signals).

I^2C Protocol

Normally, a standard communication consists of four parts:
- START signal generation
- Slave address transfer
- Data transfer
- STOP signal generation

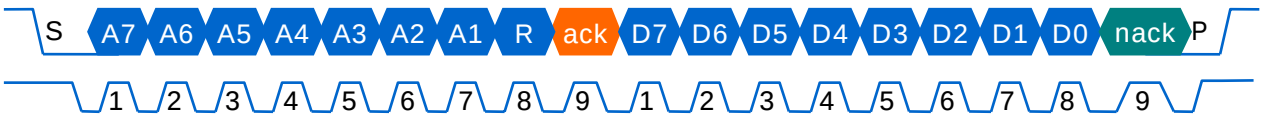


Figure 7 I^2C protocol

START Signal

When the bus is free/idle, meaning no master device is engaging the bus (both SCL and SDA lines are high), a master can initiate a transfer by sending a START signal. A START signal, usually referred to as the S-bit, is defined as a high-to-low transition of SDA while SCL is high. The START signal denotes the beginning of a new data transfer.

A Repeated START is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. from writing to a device to reading from a device) without releasing the bus.

The core generates a START signal when the STA-bit in the Command Register is set and the RD or WR bits are set. Depending on the current status of the SCL line, a START or Repeated START is generated.

Slave Address Transfer

The slave address is the first byte of data transferred by the master immediately after the START signal. This is a seven-bits calling address followed by a RW bit. The RW bit signals the slave the data transfer direction. No two slaves in the system can have the same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

Note: The core supports 10bit slave addresses by generating two address transfers. See the Philips I^2C specifications for more details.

The core treats a Slave Address Transfer as any other write action. Store the slave device's address in the Transmit Register and set the WR bit. The core will then transfer the slave address on the bus.

Data Transfer

Once successful slave addressing has been achieved, the data transfer can proceed on a byte-by-byte basis in the direction specified by the RW bit sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a No Acknowledge, the master can generate a STOP signal to abort the data transfer or generate a Repeated START signal and start a new transfer cycle.

If the master, as the receiving device, does not acknowledge the slave, the slave releases the SDA line for the master to generate a STOP or Repeated START signal.

To write data to a slave, store the data to be transmitted in the Transmit Register and set the WR bit. To read data from a slave, set the RD bit. During a transfer the core set the TIP flag, indicating that a Transfer is In Progress. When the transfer is done the TIP flag is reset, and an interrupt generated. The Receive Register contains valid data after the IF flag has been reset. The user may issue a new write or read command when the TIP flag is reset.

STOP Signal

The master can terminate the communication by generating a STOP signal. A STOP signal, usually referred to as the P-bit, is defined as a low-to-high transition of SDA while SCL is at logical '1'.

Arbitration Procedure

■ Clock Synchronization

The I^2C bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters simultaneously try to control the bus, a clock synchronization procedure determines the bus clock. Because of the wired-AND connection of the I^2C signals, a high to low transition affects all devices connected to the bus. Therefore a high to low transition on the SCL line causes all concerned devices to count off their low period. Once a device clock has gone low it will hold the SCL line in that state until the clock high state is reached. Due to the wired-AND connection the SCL line will therefore be held low by the device with the longest low period, and held high by the device with the shortest high period.

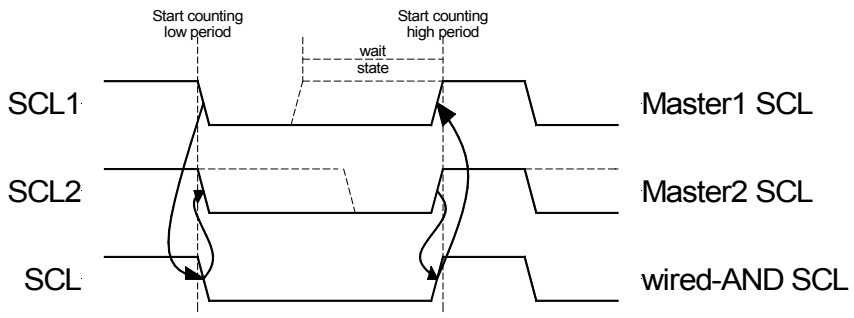


Figure 8 Arbitration Procedure

■ Clock Stretching

Slave devices can use the clock synchronization mechanism to slow down the transfer bit rate. After the master has driven SCL low, the slave can drive SCL low for the required period and then release it. If the slave's SCL low period is greater than the master's SCL low period, the resulting SCL bus signal low period is stretched, thus inserting wait-states.

GPIO interface

The ports GPIO[9:0] are general purpose IO, and used as button or LED which indicate Volume control, music paly/stop, link statues display and so on. The special function of each port can be configured by SW.

Where, GPIO[3:0] are shared for UART connections. GPIO[3:0] is used for UART transport by configuring related register by SW.

GPIO[9:0] is pull down controllable.

The PWR is voltage value high indication port and is used as Multi function port. High level (BAT voltage) of this port means button is turned on. It is used for power on, power down, page scan mode of Chip according of its high level and Duration of High level.

ELECTRICAL CHARACTERISTICS

RF Specifications

[Table 3] Receiver RF Specifications

Parameters	Mode and Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Rx Sensitivity	GFSK, 1Mbps, 0.1% BER	–	-87.0	-85.0	dBm
	DQPSK, 2Mbps, 0.01% BER	–	-89.0	-87.0	dBm
	8DPSK, 3Mbps, 0.01% BER	–	-82.0	-80.0	dBm
Maximum Input	–	–	–	10.0	dBm
Interference Performance	C/I CCI (GFSK, 0.1% BER)	–	–	11.0	dB
	C/I 1MHz ACI (GFSK, 0.1% BER)	–	–	0.0	dB
	C/I 2MHz ACI (GFSK, 0.1% BER)	–	–	-30.0	dB
	C/I ≥3MHz ACI (GFSK, 0.1% BER)	–	–	-40.0	dB
	C/I image channel (GFSK, 0.1% BER)	–	–	-9.0	dB
	C/I CCI (DQPSK, 0.1% BER)	–	–	13.0	dB
	C/I 1MHz ACI (DQPSK, 0.1% BER)	–	–	0.0	dB
	C/I 2MHz ACI (DQPSK, 0.1% BER)	–	–	-30.0	dB
	C/I ≥3MHz ACI (DQPSK, 0.1% BER)	–	–	-40.0	dB
	C/I image channel (DQPSK, 0.1% BER)	–	–	-7.0	dB
	C/I CCI (8DPSK, 0.1% BER)	–	–	21.0	dB
	C/I 1MHz ACI (8DPSK, 0.1% BER)	–	–	5.0	dB
	C/I 2MHz ACI (8DPSK, 0.1% BER)	–	–	-25.0	dB
	C/I ≥3MHz ACI (8DPSK, 0.1% BER)	–	–	-33.0	dB
	C/I image channel (8DPSK, 0.1% BER)	–	–	0.0	dB
Out-of-Band Blocking Performance (CW)	30 MHz to 2000 MHz (GFSK, 0.1% BER)	–	-10.0	–	dBm
	2000 MHz to 2399 MHz (GFSK, 0.1% BER)	–	-27.0	–	dBm
	2498 MHz to 3000 MHz (GFSK, 0.1% BER)	–	-27.0	–	dBm
	3000 MHz to 12.75 GHz (GFSK, 0.1% BER)	–	-10.0	–	dBm
Intermodulation Performance	BT, Delta f = 5MHz	-39.0	–	–	dBm

[Table 4] Transmitter RF Specifications

Parameters	Mode and Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Channel Spacing	–	–	1	–	MHz
Maximum Output Power	Class 2	-3	2	4	dBm
Output Power Range	–	-30	–	4	dBm
In-Band Spurious Emission	±500 kHz	–	–	-20.0	dBc
	1.0MHz<|M – N|<1.5 MHz (EDR only)	–	–	-26.0	dBc
	1.5MHz<|M – N|<2.5 MHz (EDR only)	–	–	-20.0	dBm
	|M – N|>2.5 MHz (EDR only)	–	–	-40.0	dBm
LO Performance	Lock time	–	100	150	us
	Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift	DH1 packet	–	±20	±25	kHz
	DH3 packet	–	±20	±40	kHz
	DH5 packet	–	±20	±40	kHz
	Drift rate	–	10	20	kHz/50us
Frequency Deviation	00001111 sequence in payload	140	160	175	kHz
	01010101 sequence in payload	115	150	165	kHz

Power Consumption

[Table 5] Power Supply Current (With a normal 3.7V battery voltage)

Operating Mode	Typical	Unit
HV3	18.0	mA
EV3	18.0	mA
2EV3	16.0	mA
A2DP Active Mode: 2DH5, 350 kbps SBC	17.6	mA
Single HFP Sniff (500ms Interval)	410	uA
Deep Sleep (off) Mode	5.0	uA

Note :
The currents are measured without an audio signal present.
The currents are measured with LEDs off.
The sniff mode current is measured with the device operating in Slave mode.
The A2DP Active mode current is with the device operating in Slave mode.

PACKAGE INFORMATION

QFN 48Pin 7x7 mm

CONTACT INFORMATION

Vimicro WuXi Headquarter

10/F 530 Tower, QingYuan Road, TaiHu International Technology Park,
WuXi New District, 214135, China
Tel: 86-510-81816000 Fax: 86- 510-81816935
WEB: WWW.VIMICRO.COM

Vimicro Beijing

16/F Shining Tower, No.35 Xueyuan Road, Haidian District, Beijing 100191, China
Tel: 86-10-68948888 Fax: 86-10-68944075

Vimicro Shanghai

2-101, Zhangjiang Micro-electronics Port, 690 Bibo Road, Zhangjiang High-tech Park,
Pudong New District, Shanghai 201203, China
Tel: 86-21-50807000 Fax: 86-21-50807611

Vimicro Shenzhen

4/F T2-B Building, South District, High-Tech Industrial Park Shenzhen 518057,
Guangdong Prov, China
Tel: 86-755-26719818 Fax: 86-755-26719539

Vimicro USA Viewtel Corporation

19447 Pauma Valley Drive, Porter Ranch , CA, 91326 USA
Tel : 1-650-966-1882 Fax : 1-650-966-1885

